IN THE CLAIMS

Please amend claims 1, 3-4, 6, 8-9, 21, and 23 as indicated below.

Please add new claims 25-36 as indicated below.

---

1. (Currently Amended) A system comprising:

a processor; and

a memory device coupled to the processor and contained within a single integrated circuit, the memory device including:

E1

a main memory;

a cache memory coupled to the processor and to the main memory to stored recently accessed data and addresses associated with the recently accessed data; and

a wait control logic coupled to the processor, the main memory, and the cache memory, ~~the wait control logic signaling~~ to signal the processor whether the data currently requested is ready to be read, the wait control logic transmitting a first signal having a duration of one clock cycle to the processor when data currently requested is in the cache memory, and the wait control logic transmitting a second signal having a duration of multiple clock cycles when the data currently requested is not in the cache memory ~~if data currently requested is not in the cache memory, to indicate that the requested data is not ready to be read, and the wait control logic signaling the processor to indicate that the requested data is ready to be read on a next processor cycle, if the requested data is in the cache memory~~.

2. (Previously Presented) The system of claim 1, wherein the memory device further comprises an address latch logic to receive the addresses of the requested data, and wherein the cache memory of the memory device further comprises:

an address cache memory coupled to the address latch logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched; and

a data cache memory coupled to the address cache memory and the main memory to store the recently accessed data, the data cache memory receiving data from the main memory if the data requested is not in the data cache memory.

3. (Currently Amended) The system of claim 2, wherein the memory device further comprises a comparator coupled to the address latch logic and the address cache memory to determine whether the address stored in the address latch logic is in the address cache memory, an output of the comparator coupling to the wait control logic to cause the wait control logic ~~asserting the signal~~ transmitting one of the first and second signals to the processor [[if]] dependent upon whether the address stored in the address latch logic is ~~not found~~ in the address cache memory.

4. (Currently Amended) The system of claim 3, wherein the comparator causes the wait control logic to assert ~~a signal having one cycle~~ the first signal to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the ~~address of the~~ requested data is found in the data cache memory.

5. (Previously Presented) The system of claim 2, wherein the address of the requested data is not presented to the main memory if the address of the requested data is found in the address cache memory.

6. (Currently Amended) An apparatus comprising:

a memory device capable of coupling to a processor through a bus, the memory device including on a single integrated circuit:

a main memory;

a cache memory coupled to the main memory storing recently accessed data and addresses associated with the recently accessed data; and

a wait control logic coupled to the main memory and the cache memory~~, the wait control logic capable of signaling~~ to signal the processor through the bus whether the data currently requested is ready to be read, the wait control logic transmitting a first signal having a duration of one clock cycle to the processor when data currently requested is in the cache memory, and the wait control logic transmitting a second signal having a duration of multiple clock cycles when the data currently requested is not in the cache memory ~~, if data currently requested is not in the cache memory, to indicate that the requested data is not ready to be read, and the wait control logic capable of signaling the processor to indicate that the requested data is ready to be read on a next processor cycle, if the requested data is in the cache memory~~.

7. (Previously Presented) The apparatus of claim 6, wherein the memory device further comprises an address latch logic to receive the addresses of the requested data, and wherein the cache memory of the memory device further comprises:

an address cache memory coupled to the address latch logic and the wait control logic to store the addresses of the recently accessed data and to store the address of the requested data after the requested data has been fetched; and

a data cache memory coupled to the address cache memory and the main memory to store the recently accessed data, the data cache memory receiving data from the main memory if the data requested is not in the data cache memory.

8. (Currently Amended) The apparatus of claim 7, wherein the memory device further comprises a comparator coupled to the address latch logic and the address cache memory to determine whether the address stored in the address latch logic is in the address cache memory, an output of the comparator coupling to the wait control logic to cause the wait control logic ~~asserting the signal~~ transmitting one of the first and second signals to the processor [[if]] dependent upon whether the address stored in the address latch logic is ~~not found~~ in the address cache memory.

E1

9. (Currently Amended) The apparatus of claim 8, wherein the comparator causes the wait control logic to assert ~~a signal having one cycle~~ the first signal to the processor to allow the processor to read in a next cycle the requested data presented by the data cache memory, if the address of the requested data is found in the data cache memory.

10-20. (Canceled)

21. (Currently Amended) The system of claim 1, wherein [[:]] the cache memory can simultaneously hold multiple non-consecutive quadwords.

22. (Canceled)

23. (Currently Amended) The apparatus of claim 6, wherein [[:]] the cache memory can simultaneously hold multiple non-consecutive quadwords.

24. (Canceled)

25. (New) The system of claim 2, wherein the memory device further comprising:

a multiplexer coupled to the data cache memory to select the requested data from the data cache memory; and

a word count control logic coupled to the address latch logic and the multiplexer to control the multiplexer to selectively output the requested data using the multiplexer.

26. (New) The system of claim 25, wherein the word count control logic receives two least significant bits of the address of the requested data, and wherein the two least significant bits are used to select up to four quadwords stored in the data cache memory to an output via the multiplexer.

27. (New) The system of claim 26, wherein the word count control logic sequentially select one of the four quadwords using information of the two least significant bits, and wherein the sequential selection is driven by a clock signal received from a bus external to the memory device.

28. (New) The system of claim 26, wherein the memory device further comprises an address counter logic coupled to the address latch logic and the main memory, and wherein the address counter logic receives the address of the requested data without two least significant bits and receives the two least significant bits of the address from the word count control logic, which when combined, selects the requested data from the main memory.

29. (New) The system of claim 3, wherein the address latch logic receives the address of the requested data without two least significant bits of the address, wherein the address cache memory stores the address without the two least significant bits.

30. (New) The system of claim 29, wherein the comparator compares the address of the requested data and the addresses stored in the address cache memory without comparing two least significant bits of the addresses.

31. (New) The apparatus of claim 7, wherein the memory device further comprising:

a multiplexer coupled to the data cache memory to select the requested data from the data cache memory; and

a word count control logic coupled to the address latch logic and the multiplexer to control the multiplexer to selectively output the requested data using the multiplexer.

32. (New) The apparatus of claim 31, wherein the word count control logic receives two least significant bits of the address of the requested data, and wherein the two least significant bits are used to select up to four quadwords stored in the data cache memory to an output via the multiplexer.

33. (New) The apparatus of claim 32, wherein the word count control logic sequentially select one of the four quadwords using information of the two least significant bits, and wherein the sequential selection is driven by a clock signal received from a bus external to the memory device.

34. (New) The system of claim 32, wherein the memory device further comprises an address counter logic coupled to the address latch logic and the main memory, and wherein the address counter logic receives the address of the requested data without two least significant bits and receives the two least significant bits of the address from the word count control logic, which when combined, selects the requested data from the main memory.

35. (New) The apparatus of claim 8, wherein the address latch logic receives the address of the requested data without two least significant bits of the address, wherein the address cache memory stores the address without the two least significant bits.

36. (New) The apparatus of claim 35, wherein the comparator compares the address of the requested data and the addresses stored in the address cache memory without comparing two least significant bits of the addresses.